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ALGORITHMIZATION OF THE FAILED SUBSCHEMES LOCALIZATION PROCESS

Abstract. *Approaches to the algorithmization of the process of localizing faulty subschemes of a wide class of electrical devices (in particular, electrical and electronic) are considered, appropriate algorithms are proposed, and the possibility of their application in practical applications is shown. In particular, it was noted that in modern conditions, with increasing requirements for the reliability of electrical devices and expanding the set of functions performed by them, not only the full feasibility of monitoring the operability of these devices at the production and operation stages should be considered, but also ensuring the potential possibility of diagnosing the developed devices (systems) - at the design stage. At the same time, the observed complication of the methodological support of individual procedures and the whole diagnostic process as a whole is indicated, which, on the one hand, is connected with the need to carry out the most complete and comprehensive diagnosis, and on the other hand, determines a sharp increase in computing resources and labor costs for the implementation of a diagnostic experiment. One of the possible solutions to this contradiction is the formalization and subsequent algorithmization of diagnostic procedures, which ensures the automation of the latter and, as a result, reduces the time of diagnosis and improves its quality. The proposed algorithmic tools implement model-oriented methods for the localization of faulty subschemes of electrical devices (systems), in particular, the method of training and testing characteristics. A distinctive feature of these methods and the algorithmic support considered in the work is the use of models of the devices under study during a diagnostic experiment, which makes it possible to form and test functionally necessary (ideally, any) health hypotheses of the latter.*

Keywords: *diagnostics, diagnostic experiment, diagnostic methods, algorithmization of diagnostic procedures, localization of faulty subcircuits*

Introduction. An important and relevant scientific and technical problem of the current level of technological development is the diagnosis of its technical condition. And, in this sense, electrical devices (ED) for various purposes are no exception [1-15]. Given the way in which the ED is involved in the process, the task of diagnosing them acquires certain features. In particular, diagnostics can be made for devices that are out of the technological cycle (disconnected), or for devices that are directly in operation (i.e., those that cannot be taken out of service under the conditions of the technological process). The latter is inherent (for example, [16, 17]) to security and alarm elements; dispatching control without reservation; offline devices, etc.

From the currently known, methods of functional and test diagnosis of ED have found wide application [1; 17-19]. A characteristic feature of these methods is the need to generate test signals at the input of diagnosed devices, form a set of hypotheses regarding the performance of the latter, as well as analyze the results of testing accepted hypotheses. At the same time, on the one hand, the routine and laboriousness of carrying out diagnostic procedures (drawing up test signals, sequentially looking through them during a diagnostic experiment, obtaining measurement results of their analysis) are obvious, and, on the other hand, the possibility of algorithmic stages of a diagnostic study. Algorithmization, in this case, automates the diagnostic experiment, which, in turn, increases its efficiency, since in the automatic mode you can create a complete set of test signals for which you can perform the necessary measurements and process their results, reduce the time of diagnosis, and optimize the number of personnel involved in the diagnostic experiment.

Thus, it becomes clear the relevance of research related to the algorithmization of the process of diagnosing ED, in particular, the localization of faulty subschemes.

Objective of the study. Development of approaches to the algorithmization of procedures for the localization of faulty subschemes in the diagnosis of ED.

The main description of the study. As a methodological basis for the algorithmization of ED diagnostic procedures for the localization of faulty

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subcircuits, we use the method of training and verification characteristics (TVC), which was described in detail in [20-23]. We only note that the TVC method is based on obtaining estimates of the input and output signals of the checked subcircuit, and various properties of the checked subcircuit are analyzed: independent observability, independent controllability, independent observability and controllability.

1. The main stages of the localization of faulty subschemes in electronic devices. The general algorithm for applying the TVC method to localize faulty subcircuits is shown in Fig. 1.

It includes the following steps [20-23]:

– dividing the circuit into subschemes (subcircuits);

– formation of hypothesis testing sequence;

– hypothesis testing;

– analysis of the results of testing hypotheses.

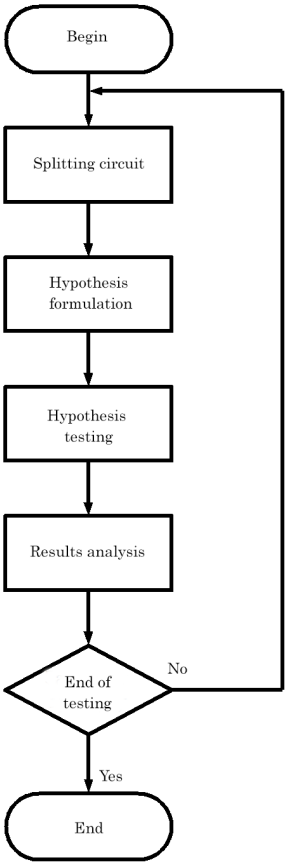


Fig. 1. General algorithm for applying the TVC method to localize faulty subcircuits

When automating the breaking of a circuit into subcircuits, it is necessary to solve problems related to the storage in the computer memory of information on the electrical circuit topology, the development of an algorithm for partitioning it into subcircuits and extracting typologically indistinguishable subschemes.

The formation of a sequence of testing hypotheses should be based on the analysis of the results of testing previous hypotheses and the distinguishability of subcircuits. As a result, the area containing the fault should be determined as accurately as possible.

Algorithmization of hypothesis testing can be achieved by using existing (or developing new) electrical circuit simulation programs.

2. Forming a sequence of testing hypotheses Method TVC, as mentioned above, is to test the hypotheses one by one about the failure of the ED subschemes. At the same time, an important restriction on the tested subcircuits is the number of their pole nodes, which should not be greater than the number of measured signals. Since the number of subcircuits obtained as a result of partitioning a circuit into subcircuits, with such a restriction can be quite large, then the enumeration of all the hypotheses turns out to be very laborious. Therefore, it is advisable to form a sequence of testing hypotheses to avoid step-by-step examination of all subcircuits.

The most natural is such a sequence of testing hypotheses, in which the largest in some sense subcircuits are first checked, after determining a faulty one, the largest ones embedded in it are checked, etc. In other words, a directed search of a faulty area is achieved.

We introduce the concept of *subcircuit size* and *nesting* relations between them. Let the electrical circuit of an electrical device be specified using graph $G(V, E)$, where V and E are the sets of vertices and edges of the graph, respectively. Then subcircuit S_i will correspond to subgraph $G_i^0(V_i^0, E_i^0)$, and the rest of the circuit will correspond to $G_i^0(V_i^0, E_i^0)$ such that

$$V_i \subset V;\ V_i^0 \subset V;\ V_i \bigcup V_i^0 = V;\ V_i \bigcap V_i^0 = V_i^p, \quad (1)$$

$$E_i \subset E;\ E_i^0 \subset E;\ E_i \bigcup E_i^0 = E;\ E_i \bigcap E_i^0 = \phi, \quad (2)$$

where: V_i^p is the set of pole nodes of the subcircuit S_i.

We divide the set of training nodes $N_{об}$ into two subsets:

$$N_{об_i}^1 \subset V_i^0,$$

$$N_{об_i}^2 \subset V_i,$$

$$N_{об_i}^1 \bigcup N_{об_i}^2 = N_{об}.$$

Then the number of poles of the subcircuit S_i must satisfy the conditions:

$$\mathrm{card} V_i^p - 1 \le \mathrm{card} N_{об_i}^1, \quad (3)$$

where: $N_{об_i}^1 \bigcap N_{об_i}^2 = \phi$.

We denote by $M^* = \{S_i\}$ the set of all possible subschemes of the circuit under test. Such a set can be obtained, for example, by considering various combinations of nodes. Selecting from M^* a subcircuit satisfying (3), we obtain a set M of subcircuits that can be checked with the available set of nodes

$$M = \{S_i : \mathrm{card} V_i^p - 1 \le \mathrm{card} N_{об_i}^1\}.$$

Consider the edge of the graph $e = (v_j; v_k)$. . From (1) and (2) it follows that,

$$\text{if } e \in E_i, \text{ then } v_j \in V_i, v_k \in V_i,$$

$$\text{if } e \in E_i^0, \text{ then } v_j \in V_i^0, v_k \in V_i^0. \quad (4)$$

In other words, with such a definition, a subscheme S_i is completely determined by the vertices of its graph, i.e.

if $v_j \in V_i,\ v_k \in V_i$, then $y = (v_j; v_k) \in E_i$. (5)

Most elements of ED can be represented using bipolar elements connected in accordance with their equivalent circuits [24; 25]. However, the splitting of circuits into subcircuits must be done without splitting the replacement circuits into their component parts, since it is physically possible to replace only the entire faulty element.

For ED circuits containing multipolar elements, instead of the notion of a branch, we will use the concept of an element characterized by the fact that it may be incident to more than two nodes. Then we assume that the element $e = (v_j, ..., v_k)$ is included in the subcircuit S_i, if $\forall v_{jr} \in V_i$. Otherwise, $e \in S_i^0$. That is, the composition of a subcircuit S_i in a circuit containing multipolar elements will also be completely determined by the set of its nodes V_i.

By the size μ_i of a subcircuit S_i we mean the number of its nodes, namely:

$$\mu_i = \text{card} V_i .$$

We say that a subcircuit S_i is larger than a subcircuit S_j if

$$\mu_i > \mu_j .$$

Подсхему S_j будем называть вложенной в подсхему S_i, если

A subcircuit S_j will be called nested (embedded) in a subcircuit S_i if

$$V_j \subset V_i,\ V ,$$

and we will designate it as $S_j \subset S_i$.

It's obvious that $\mu_i < \mu_j$.

The union of subschemes S_i and S_j will be called a subschema S_k, such that

$$V_i \bigcup V_j = V_k$$

and we will designate it as $S_k = S_i \bigcup S_j$.

The intersection of subschemes S_i and S_j will be called a subschema S_k, such that

$$V_i \bigcap V_j = V_k$$

and we will designate it as $S_k = S_i \bigcap S_j$.

It's obvious that

$$S_i \bigcup S_j \subset M^*,$$

$$S_i \bigcap S_j \subset M^*.$$

However, these relations are not satisfied for the set M, which is connected with the necessity of fulfilling condition (3).

It should be noted that if $S_j \subset S_i$, then fault of S_j entails fault of S_i.

Therefore, subcircuits S_j and S_i are indistinguishable with respect to the set of training nodes $N_{\text{об}}^1$. In other words, nesting of two subcircuits is a sufficient condition for their indistinguishability. This avoids testing hypotheses for a group of obviously indistinguishable subcircuits. Thus, it is first necessary to test the hypotheses about the failure of the largest subcircuits. These subcircuits form a set of $M_0 \subset M$ such that

$$M_0 = \{S_i : \forall i \, \overline{\exists} S_k \subset M \ S_i \subset S_k, i \neq k\}, \quad (6)$$

i.e. S_i are no longer nested in any other subcircuits of M.

After determining the faulty subcircuit, hypotheses are tested for the largest subcircuits nested in it, which form the set M_i:

$$M_i = \{S_j : \forall j \, \overline{\exists} S_k \subset M_i \ S_j \subset S_k, \ j \neq k\},$$

i,e, S_j are no longer nested in any other subcircuits of M_i.

When testing hypotheses at each stage of the splitting, the following outcomes are possible.

Case 1. One hypothesis is accepted. In this case, a defected subcircuit is divided into maximally large subcircuits, and hypotheses are tested for them.

Case 2. Accepted several hypotheses about the failure of intersecting subcircuits, having a common part, which is considered a failure zone. In this case, one of the faulty subcircuits is divided into the largest nested subcircuits, and the hypotheses are tested for those subcircuits that intersect with the malfunction zone.

Case 3. Accepted several hypotheses about the failure of subcircuits that do not have one common part for all of them. In this case, all subschemes corresponding to the accepted hypotheses are split, and the results of the tested hypotheses are considered together.

Case 4. None of the hypotheses under consideration is accepted. In this case, the localization process ends with a statement of malfunction of the subcircuits obtained in the previous partitioning step.

The block diagram of the malfunction localization algorithm is shown in Fig. 2

The use of numerical methods for solving systems of equations determines the specificity of the decision-making algorithm for each hypothesis. As a result of the simulation of the scheme when testing a hypothesis, the solution may converge or diverge. If the solution converges, then by the calculated values of the estimates of the values of the test signals we conclude that the hypothesis under consideration is accepted or dropped.

The reason for the discrepancy in the decision process may be either the non-conformity of the actual malfunction hypothesis itself (which corresponds to discarding the hypothesis) and the unsuccessfully chosen initial approximation used in the simulation. Therefore, a search is first carried out for a faulty subcircuit, and only those hypotheses are analyzed for which a solution can be obtained. If the fault localization accuracy is unsatisfactory, then the initial approximation changes or

other numerical methods are used, and an attempt is made to obtain a solution for other hypotheses that, if successful, are included in the consideration.

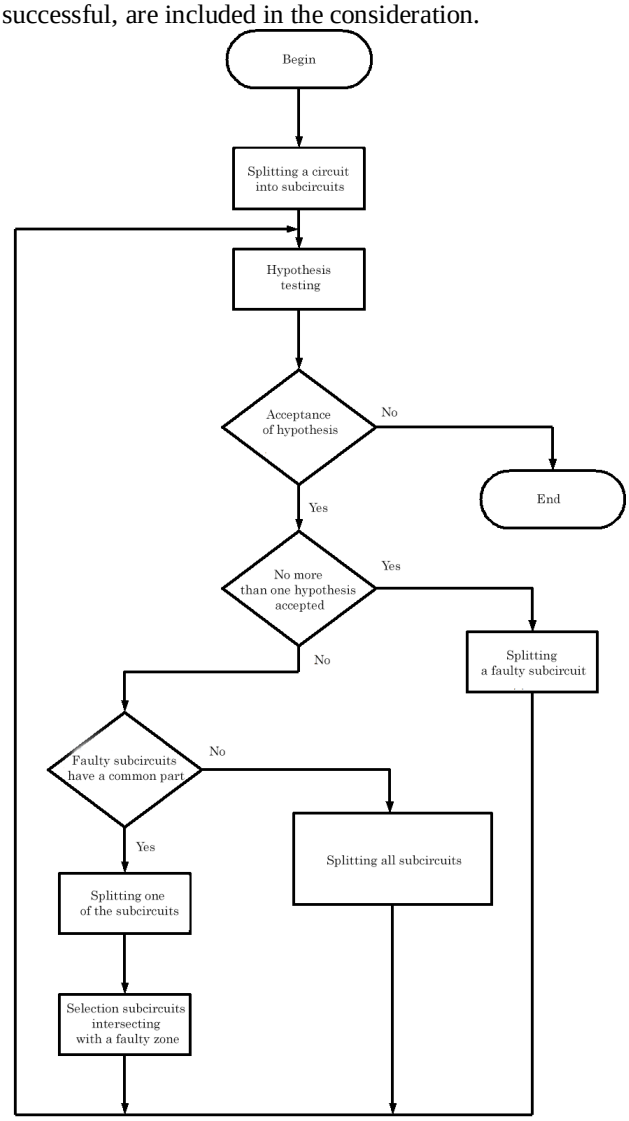


Fig. 2. Block diagram
of the malfunction localization algorithm

3. Splitting the circuit into subcircuits. Let us consider in more detail the algorithm of "splitting"" the EC scheme into subcircuits.

3.1. Formulation of the problem. In the process of applying the TVC method, it is necessary to repeatedly partition the circuit or its part into subcircuits satisfying conditions (3). This task is reduced to the problem of partitioning the graph representing the ED scheme into pairs of subgraphs $G_i(V_i, E_i)$ and $G_i^0(V_i^0, E_i^0)$. Graph splitting is widely used in the design of electronic equipment to minimize the connections between individual blocks [5; 26], optimize computational processes [27], and diagnostics of ED [28]. However, in the literature there is no problem of obtaining all possible partitions that satisfy condition (3). To solve this problem, the method of direct item-by-item examination of various subcircuits was chosen. Since the subcircuit in this definition is completely determined by its nodes, then the solution of the problem is reduced to the consideration of all possible combinations of the vertices of the graph. For large schemes, the direct application of the method of direct search of graph nodes is inapplicable, since the time spent on enumerating all the combinations depends exponentially on the number of nodes.

In addition, it should be noticed that the composition of modern electrical devices include such multi-polar elements as semiconductor transistors, integrated circuits, etc., which are impossible and impractical to break into subcircuits, and should be considered as a whole. Consequently, it is necessary in the computer to store and process information about the graph of a circuit containing multipolar elements.

Thus, to achieve the goal it was necessary to solve the following tasks:

– develop a heuristic algorithm to avoid the exponential dependence of the solution time on the number of nodes and giving a quasi-finite solution,

– to develop ways of presenting in computer memory a graph of an electrical circuit containing multipolar elements, and automating its partitioning,

– develop an algorithm for analyzing subschemes in order to form a hypothesis testing sequence.

3.2. Heuristic algorithm for splitting the graph of a chain. To reduce the number of considered subcircuits, one can limit oneself to only connected subcircuits, and to exclude the exponential dependence of the solution time of the problem of partitioning a circuit into subcircuits, a heuristic algorithm was developed. This algorithm is based on the fact that the division into subcircuits, their analysis and the selection of maximally large subcircuits is performed not for the whole circuit, but for its individual parts, called *blocks*. In this case, only a quasi-finite solution is obtained, i.e. some maximally large subcircuits will not be considered, however, malfunctions arising in practice, as a rule, can be localized with this approach. In order to lose fewer subcircuits, the selecting blocks should be intersected, then subcircuits containing nodes from different blocks will be considered (Fig. 3).

Suppose that for block 1 a complete analysis of all combinations of nodes has been carried out. Then, for block 2 intersecting with block 1, there is no need to iterate over the combinations of all the nodes, and only nodes that do not belong to block 1 should be iterated along with combinations of these nodes with subcircuits of the common part of the blocks obtained from the analysis of block 1. Block 1 in this case called base for block 2.

The given heuristic algorithm requires storing in the computer RAM only information about the current unit of the electrical circuit, which leads to memory savings.

Obviously, on the basis of this heuristic algorithm, it is possible to develop a program for analyzing the topology of an electrical circuit in units for selecting connected subcircuits and recording information about them into memory.

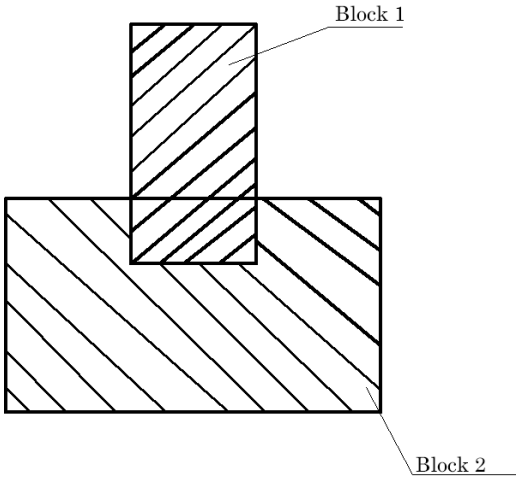


Fig. 3. Blocks with intersecting subcircuits

It is also possible to develop a program of analyzing multipole circuit according to blocks for distinguishing indistinguishable multipoles and forming a sequence of testing hypotheses.

3.3. Analysis of subcircuits and the formation of the sequence of their verification. The analysis of the subcircuits of a block is reduced to the analysis of their nesting, the determination of the largest subcircuits, and, on this basis, to the formation of a sequence of testing hypotheses.

The relationship between subcircuits on the basis of their nesting into each other can be represented as a directional graph without contours, which is explained by the transitivity of the inclusion relation (as shown in Fig. 4). Each vertex of such a graph corresponds to a subscheme. The arrow points from S_i to S_j if $S_j \subset S_i$.

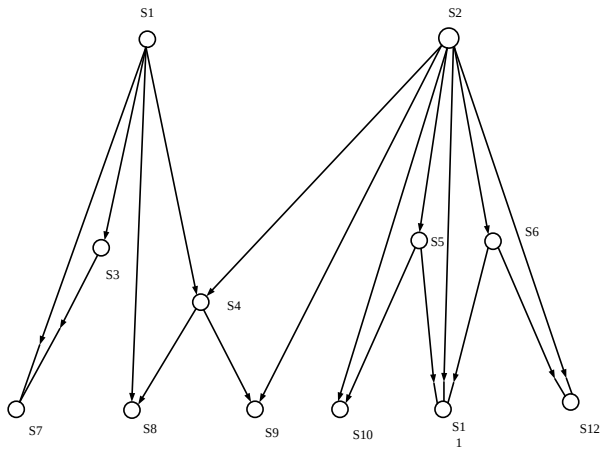


Fig. 4. Directed graph without contours

If such a graph is constructed, i.e. relations between all subcircuits are determined, then the maximally large subcircuits considered at any stage of the partitioning are at the same level, i.e the task of determining the largest subschemes is reduced to determining the levels of a graph without contours [21; 29]. For this, each vertex is assigned a number of input and output edges. If the vertex has no input edges, then this is the 1st layer. It is removed from the graph, then for all vertices for which the remote vertices were ancestors, the number of input edges is reduced by the corresponding number. Vertices that do not have input edges are searched again, and so on.

This algorithm can be simplified, given that if $S_i \subset S_j$, then $\mu_i < \mu_j \ \ (i \neq j)$, i.e., it is not necessary to view all subcircuits, but only those that have a smaller number of branches.

In the case of writing a program of analysis of multipoles through the block allocation indistinguishable multipoles according to the criterion of nesting and the formation of a sequence of testing hypotheses, the source data for this program will be the number of the analyzed block and the corresponding file.

The program should consist of the following main procedures: $prep(\cdot)$, $mpread(\cdot)$, $sort(\cdot)$, $analys(\cdot)$, as well as a number of procedures that perform service functions.

Procedure $prep(\cdot)$ performs preparatory operations for the program.

Procedure $mpread(\cdot)$ is designed to read information about a block and all its subcircuits from a file into RAM.

Procedure $sort(\cdot)$ is designed to sort multipoles by descending number of nodes in them. For this, the bubble method is used [22].

Procedure $analys(\cdot)$ performs topological sorting of subcircuits, giving the experimenter information about the largest subcircuits nested in the given one.

4. Hypothesis testing using a simulator. To automate hypothesis testing, it is proposed to use an electronic circuit simulation program. In this program, based on the input description of the electronic circuit, the Jacobi matrix is formed, which is stored in rows in a one-dimensional array $g[\cdot]$, and the vector of residuals, which is stored in an array $SS[\cdot]$. The number of equations in the system is determined by the value of the variable *keg*.

1. The following arrays are entered:

– $ncnt[\cdot]$ to store numbers of training nodes,

– $ncnc[\cdot]$ to store numbers of test nodes,

– $et[\cdot]$ to store the values of voltages in the training nodes,

– $ec[\cdot]$ to store the values of voltages in the test nodes,

– $hip[\cdot]$ to store the numbers of poles of the tested subcircuit,

- $I[\cdot]$ to store the values of current sources connected to the poles of the tested subcircuit.

2. Dialogue procedures are introduced to set the values of arrays $ncnt[\cdot]$, $ncnc[\cdot]$, $et[\cdot]$, $ec[\cdot]$, $hip[\cdot]$, and zero values are assigned to the array $I[\cdot]$ elements.

The simulator works as follows:

– the simulator calculates the Jacobi matrix $g[\cdot]$ and the magnitudes of the discrepancy $SS[\cdot]$;

– in accordance with the information entered, the number of equations keg is changed by an amount equal to the number of polar nodes of the tested subschema minus

one (the old keg value is stored in variable $keg1$);

– carried out "moving apart" the rows of the Jacobi matrix in array $g[\cdot]$ and adding to it new rows;

– the new rows and columns of the Jacobi matrix are filled in accordance with the hypothesis under consideration;

– recalculation carried of the elements of the array $SS[\cdot]$ of residuals in accordance with the hypothesis under consideration and the values of the elements of the arrays $I[\cdot]$ and $et[\cdot]$;

– control is transferred to a modeling subprogram that monitors the values of the discrepancies in order to determine the accuracy of the solution obtained and the possibility of terminating the calculations;

– the resulting arrays $g[\cdot]$, $SS[\cdot]$ and variable keg are transferred to procedure $lin(\cdot)$, which solves the system of linear algebraic equations and returns the values of the increments of variables in array $SS[\cdot]$. At the same time, the variables of the original system of equations are corrected;

– adjustment carried of the elements of the array $I[\cdot]$ to the corresponding values of the increments;

– the old value of $keg1$ is restored from keg, and proceeds to step 1.

Below is described the localization of faulty subschemes in practical circuits on the example of a power amplifier.

The circuit diagram of the power amplifier is shown in Fig. 5, and the numbering sequence of its elements in the Table 1. The nodes 2; 3; 4; 6 are available in the scheme. In Table 2 shows the voltage values in the available nodes for the case of a working circuit and for the case of a malfunction that must be determined.

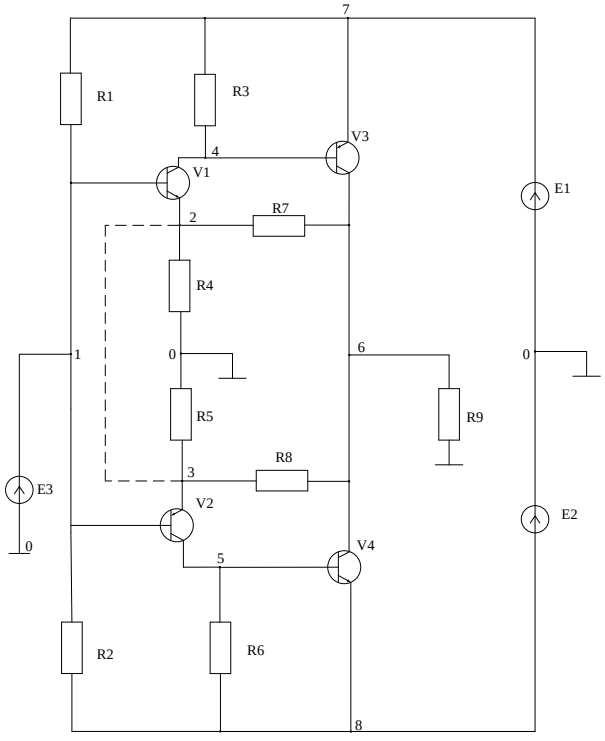


Fig. 5. Schematic diagram of the power amplifier

Table 1. Numbering of elements of the power amplifier concept

Item No.	Reference designations	Value
1	*E*1	15 V
2	*E*2	15 V
3	*R*1	10 kΩ
4	*R*2	10 kΩ
5	*R*3	270 ohm
6	*R*4	47 ohm
7	*R*5	47 ohm
8	*R*6	270 ohm
9	*R*6	270 ohm
10	*R*8	270 ohm
11	*V*1	CT 503 V
12	*V*2	CT 502 V
13	*V*3	CT 816 V
14	*V*4	CT 817 V
15	*R*9	4 ohm
16	*E*3	1 V

Table 2. Voltage values in the available nodes

Item No.	Voltage	
	Fault-free circuit	Faulty circuit
2	0,605	0,6
3	0,311	0,6
4	17,493	17,491
6	2,1	2,305

The localization of a faulty subcircuit is performed in the following sequence:

– a conclusion is made about the efficiency of EMF sources $E1$, $E2$, $E3$;

– the power amplifier circuit is divided into subcircuits. As available nodes, nodes with numbers 2; 3; 4; 6 are entered, and the scheme itself is considered to consist of one block. The results of the partition for the first level are given in Table. 3;

Table 3. Hypotheses for tested subcircuits

Subcircuit No.	Poles	Subcircuit No.	Poles
2	0,1,3,6	29	0,3,4,7
5	0,1,4,6	30	0,2,7,8
7	3,4,6,7	31	0,2,6,8
8	2,5,6,8	32	0,2,6,7
9	2,4,6,7	33	0,2,5,8
10	1,5,7,8	34	0,2,4,7
12	1,4,7,8	35	0,2,3,8
15	1,3,5,7	36	0,2,3,7
17	1,2,4,8	37	0,2,3,6
18	1,2,4,7	38	0,1,7,8
19	1,2,4,6	44	0,1,3,7
20	0,6,7,8	47	0,1,2,8
21	0,5,7,8	48	0,1,2,7
23	0,4,7,8	49	0,1,2,6
25	0,3,7,8	50	0,1,2,4
27	0,3,6,7	51	0,1,2,3

– using a modified simulation program, hypotheses are checked for all the subcircuits listed in Table. 4.3, along with this nodes 2; 3; 6 are taken as training nodes, and node 4 is used as a test node. As a result of the simulation, a single hypothesis is confirmed, corresponding to subschema 37 with pole nodes 0; 2; 3; 6

$$\delta_{37} = \left|U_4 - \hat{U}_4\right| = 2 \cdot 10^{-6}\ B;$$

– the results of partitioning (for example) of the subcircuit 37 are given in table four.

Table 4

Subcircuit breakdown results 37

Subcircuit No.	Poles
54	2,3,6
67	0,3,6
70	0,2,6
71	0,2,3

- using a simulator, hypotheses can be tested for all subcircuits shown in Table 4, moreover, nodes 2 and 3 are taken as training nodes, and node 6 is taken as a test node. As a result of the simulation, two hypotheses are confirmed, corresponding to subschemes 54 and 71

$$\delta_{54} = \left|U_6 - \hat{U}_6\right| = 0{,}062V,$$
$$\delta_{71} = \left|U_6 - \hat{U}_6\right| = 0{,}059V,$$

– since subcircuits 54 and 71 have common nodes, a part of these subcircuits, which consists of nodes 2 and 3, is taken as a fault zone. This part does not contain elements and is not subject to further splitting. This result corresponds to the actual fault depicted by the dotted line in Fig. 5. The given example shows a relatively low computational complexity of the proposed algorithm for the localization of faulty subcircuits.

Conclusions. On the basis of the developed algorithms (Fig. 1; Fig. 2), the method of localization of faulty subschemes in the ED is considered, which includes the following sequence of actions:

1. The scheme of the checked ED is divided into subcircuits taking into account the number and location of nodes available for measurements.

2. Based on the topological indistinguishability criterion, groups of indistinguishable subcircuits are determined.

3. For ED circuits containing only linear elements, using a simulation program, a fault vocabulary is constructed for the resulting subcircuit partitioning, and it determines the faulty subcircuit with an accuracy of indistinguishable subcircuits.

4. In the ED circuits containing nonlinear elements, for each subcircuit being tested, the nodes available for measurement are divided into two groups, namely, into training and testing nodes. If the hypothesis about the malfunction is confirmed, only for one of the considered subcircuits, in order to increase the depth of diagnosis, the composition of the control points is changed, and the transition to step 1.

If the hypothesis about the malfunction of several of the considered subcircuits having a common part is confirmed, the composition of the control points is changed to increase the depth of diagnosis, and the transition to step1 is carried out.

When confirming the hypotheses about the failure of several subcircuits that do not have a common part, a subcircuit representing the union of these subcircuits is taken, the composition of control points is changed, and the transition to step 1 is made. When discarding the failure hypotheses for all the subcircuits considered, the process of searching for a malfunctioning subcircuit ends, and that subcircuit that was determined at the previous stage is considered to be faulty.

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АЛГОРИТМІЗАЦІЯ ПРОЦЕСУ ЛОКАЛІЗАЦІЇ НЕСПРАВНИХ ПІДСХЕМ

Анотація *Розглянуто підходи щодо алгоритмізації процесу локалізації несправних підсхем широкого класу електротехнічних пристроїв (переважно електричних та електронних), запропоновано відповідні алгоритми та показано можливість їх прикладного застосування в практичних додатках. Зокрема, зазначено що в сучасних умовах, при зростанні вимог до надійності електротехнічних пристроїв та розширення набору функцій, які вони виконують, повинна розглядатися не тільки повна можливість реалізації поточного контролю працездатності даних пристроїв на стадіях виробництва та експлуатації, але й забезпечення потенціальної можливості діагностування пристроїв (систем) – на стадії проектування. Разом з тим вказано на ускладнення, яке спостерігається, щодо методологічного забезпечення окремих процедур та всього процесу діагностування в цілому, що, з одного боку, пов'язано з необхідністю найбільш повно та всебічно провести діагностування, а з іншого – визначає різке зростання обчислювальних ресурсів та трудовитрат на реалізацію діагностичного експерименту.*

Одним з можливих рішень вказаного протиріччя слугує формалізація та наступна алгоритмізація процедур діагностування, що забезпечує автоматизацію останніх та, як наслідок, скорочує час діагностування і підвищує його якість. Запропоновані алгоритмічні засоби реалізують модельно-орієнтовані методи локалізації несправних підсхем електротехнічних пристроїв (систем), зокрема, метод навчаючих та перевірочних характеристик. Відмінною особливістю даних методів та розглянутого в роботі алгоритмічного забезпечення є використання в ході діагностичного експерименту моделей пристроїв, які досліджуються, що забезпечує можливість формування та перевірки функціонально необхідних (в ідеалі – будь-яких) гіпотез працездатності останніх.

Ключові слова: *діагностування; діагностичний експеримент; методи діагностування; алгоритмізація процедур діагностування;, локалізація несправних підсхем*

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АЛГОРИТМИЗАЦИЯ ПРОЦЕССА ЛОКАЛИЗАЦИИ НЕИСПРАВНЫХ ПОДСХЕМ

Аннотация *Рассмотрены подходы к алгоритмизации процесса локализации неисправных подсхем широкого класса электротехнических устройств (преимущественно электрических и электронных), предложены соответствующие алгоритмы и показана возможность их прикладного применения в практических приложениях. В частности отмечено, что в современных условиях, при возрастании требований к надежности электротехнических устройств и расширения набора, выполняемых ними функций, должна рассматриваться не только полная реализуемость текущего контроля работоспособности данных устройств на стадиях производства и эксплуатации, но и обеспечение потенциальной возможности диагностирования разрабатываемых устройств (систем) – на стадии проектирования. Указано вместе с тем на наблюдающееся усложнение методологического обеспечения отдельных процедур и всего процесса диагностирования в целом, что, с одной стороны, связано с необходимостью наиболее полно и всесторонне провести диагностирование, а с другой – определяет резкое возрастание вычислительных ресурсов и трудозатрат на реализацию диагностического эксперимента.*
Одним из возможных решений указанного противоречия служит формализация и последующая алгоритмизация процедур диагностирования, что обеспечивает автоматизацию последних и, как следствие, сокращает время диагностирования и повышает его качество. Предложенные алгоритмические средства реализуют модельно-ориентированные методы локализации неисправных подсхем электротехнических устройств (систем), в частности, метод обучающих и проверочных характеристик. Отличительной особенностью данных методов и рассмотренного в работе алгоритмического обеспечения является использование в ходе диагностического эксперимента моделей исследуемых устройств, что обеспечивает возможность формирования и проверки функционально необходимых (в идеале — любых) гипотез работоспособности последних.

Ключевые слова*: диагностирование; диагностический эксперимент; методы диагностирования; алгоритмизация процедур диагностирования; локализация неисправных подсхем*